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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,193	08/18/2003	Azeez Bhavnagarwala	YOR920030289US1 (8728-635)	3651
46069 7590 07/22/2011 F. CHAU & ASSOCIATES, LLC Frank Chau 130 WOODBURY ROAD WOODBURY, NY 11797			EXAMINER WEST, JEFFREY R	
			ART UNIT 2857	PAPER NUMBER
			NOTIFICATION DATE 07/22/2011	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No. 10/643,193	Applicant(s) BHAVNAGARWALA ET AL.	
	Examiner Jeffrey R. West	Art Unit 2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 May 2011.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 10-13, 18, 19, 27, 29, 32-34 and 38 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 10-13, 18, 19, 27, 29, 32-34 and 38 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 October 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114 was filed in this application after a decision by the Board of Patent Appeals and Interferences, but before the filing of a Notice of Appeal to the Court of Appeals for the Federal Circuit or the commencement of a civil action. Since this application is eligible for continued examination under 37 CFR 1.114 and the fee set forth in 37 CFR 1.17(e) has been timely paid, the appeal has been withdrawn pursuant to 37 CFR 1.114 and prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on May 23, 2011, has been entered.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

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Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 10-13, 18, 19, 27, 29, 32-34, and 38 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

It has been held that the first step in determining whether a claim recites patent eligible subject matter is to determine whether the claim falls within one of the four statutory categories of invention recited in 35 USC § 101: process, machine, manufacture and composition of matter. The latter three categories define "things" or "products," while a "process" consists of a series of steps or acts to be performed. For purposes of § 101, a "process" has been given a specialized, limited meaning by the courts.

Claims 10-13, 18, and 19 are only drawn to a process that is not tied to another statutory class, either explicitly or inherently, and does not perform any physical transformation. Additionally, the claims are drawn to an abstract idea and there is no evidence of record indicating that the claims are only limited to a practical application of the abstract idea. As such, claims 10-13, 18, and 19 are drawn to non-statutory subject matter.

Claims 27, 29, 32-34, and 38 are drawn to a "program storage device". The broadest reasonable interpretation of a claim drawn to a program storage device covers forms of non-transitory tangible media and transitory propagating signals *per se* in view of the ordinary and customary meaning of computer readable media, particularly when the specification is silent (see MPEP 2111.01). Because the

broadest reasonable interpretation covers a signal *per se*, a rejection under 35 USC 101 is appropriate as covering non-statutory subject matter. See 351 OG 212, Feb 23 2010.

The Examiner suggests that Applicant amends the claims as follows: “program storage device...embodying a program of instructions executable by the machine to perform” should be ---non-transitory program storage device... embodying a program of instructions that when executed by the machine performs---.

Response to Arguments

5. Applicant's arguments with respect to claims 10-13, 18, 19, 27, 29, 32-34, and 38 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.

U.S. Patent No. 6,275,094 to Cranford, Jr. et al. discloses a method for characterizing device mismatch in a semiconductor integrated circuit, comprising the steps of obtaining DC voltage characteristic data for a device pair comprising first and second semiconductor transistor devices (column 7, lines 4-9) wherein the DC voltage characteristic data comprises an output DC voltage (column 7, lines 7-9 and column 8, lines 1-4) as a function of an input DC voltage (column 7, lines 14-16) wherein the input voltage is applied to a gate of at least one of the first and second

semiconductor transistors (column 7, lines 14-16) and wherein the output voltage is obtained at a common node connection of the first and second semiconductor transistor devices (column 7, lines 7-9) and processing the DC voltage characteristic data to determine a distribution of device mismatch between the semiconductor devices (column 7, lines 20-23 and 28-36).

Conti et al., "Test structure for mismatch characterization of MOS transistors in subthreshold regime". teaches a test structure for threshold voltage mismatch comprising obtaining subthreshold DC voltage characteristic data for adjacent transistor devices (page 173, column 1, "Introduction, lines 1-9 and page 173, column 2, "Mismatch Model", lines 9-13) by biasing the transistors in a subthreshold region through application of corresponding gate voltages (page 173, "Test Circuits" and page 174, column 1, lines 1-7).

U.S. Patent No. 6,731,916 to Haruyama teaches a power amplifying apparatus for a mobile phone including an FET with a bias current setting circuit (column 3, lines 9-11) and a memory/database (column 3, lines 11-13) wherein voltage characteristic data for the FET is stored in the memory/database (column 3, lines 14-20) and, when needed, is retrieved from the memory/database (column 3, lines 42-47).

U.S. Patent No. 5,999,043 to Zhang et al. teaches an on-chip high resistance device for passive low pass filters with programmable poles comprising a transistor device that is controlled to operate in a subthreshold region through variation in the voltage applied to the gate (column 3, lines 46-49).

U.S. Patent No. 6,819,183 to Zhou et al. teaches temperature and process compensation of MOSFETs operating in sub-threshold mode wherein a level of a current source is set to maintain a gate voltage of the MOSFET at a constant below its threshold voltage, thereby maintaining operation in a subthreshold region (column 6, lines 17-21).

U.S. Patent No. 4,851,768 to Yoshizawa et al. teaches a characteristic test apparatus for an electronic device comprising a transistor pair configured with a node for measuring an output voltage, that varies as a function of the input voltage, between the first and second transistors (Figure 2a) wherein a varying/distribution of input voltages are applied to obtain voltage output to determine a threshold voltage as part of a DC voltage characteristic (column 4, lines 59-67) wherein the threshold voltage can be determined either by determining the distribution of input voltages for a given output voltage or determining a distribution of output voltages for a given input (column 6, lines 6-17).

U.S. Patent No. 6,181,621 to Lovett teaches a threshold voltage mismatch compensated sense amplifier for SRAM memory arrays comprising means for obtaining threshold voltage mismatch information in a SRAM (column 1, lines 6-10 and column 2, lines 7-15).

U.S. Patent No. 6,798,278 to Ueda teaches a voltage reference generation circuit and power source incorporating such a circuit wherein a variation in threshold voltage mismatch is determined for a transistor pair by determining a standard deviation (column 13, lines 28-41).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey R. West whose telephone number is (571)272-2226. The examiner can normally be reached on Monday through Friday, 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Schechter can be reached on 571-272-2302. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jeffrey R West/
Primary Examiner, Art Unit 2857

July 19, 2011